



# Test and Debug Challenges for PCIe® 4.0

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# Disclaimer



**Presentation Disclaimer: All opinions, judgments, recommendations, etc. that are presented herein are the opinions of the presenter of the material and do not necessarily reflect the opinions of the PCI-SIG®.**

# Agenda



- **PCIe Overview including what's new with PCIe<sup>®</sup> 4.0**
- **PCIe Transmitter Testing**
- **PCIe Receiver Testing**
- **PCIe 4.0 Rx Debug Use Case**

# PCIe Compliance Testing



- **PCI-SIG holds regular Compliance Workshops typically 4x/yr**
- **Vendors who desire to be on PCI-SIG Integrator's List attend PCI-SIG workshops where they must pass all four electrical tests & 80% of interoperability tests**

## PCIe 3.0 Electrical PHY Compliance Tests

Transmitter Testing

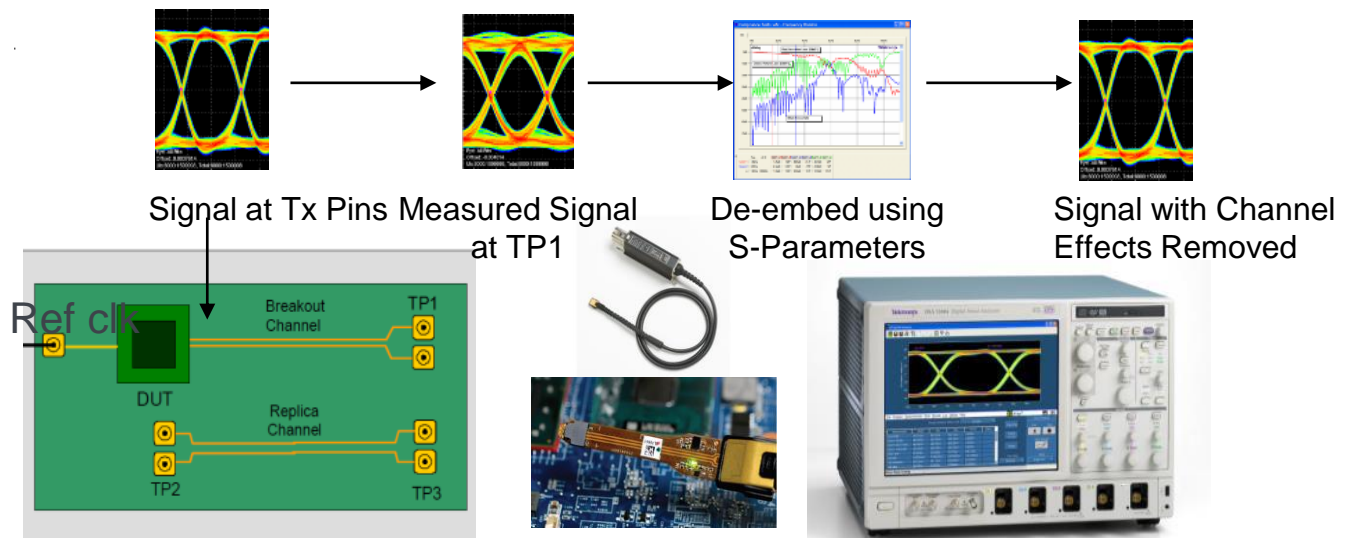
Receiver Jitter Tolerance Testing

Tx/Rx Link Equalization Testing

PLL Loop Bandwidth Testing

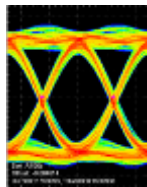
# Base Spec Tx Testing

- **Base Specification Measurements** are defined at the pins of the transmitter
- **Signal access at the pins is often not possible**
- **De-embedding** is required to see what the signal looks like at the pins of the TX, without the added effects of the channel
- **S-Parameters** are acquired on the replica channel
- **Measurement at TX pins can also be enabled by high fidelity probes, eg P7700**

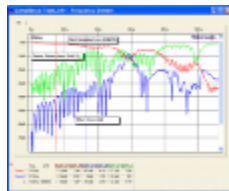


# CEM & U.2 Spec Tx Testing

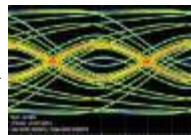
- **CEM Specification Measurements are defined at the slicer of a receiver**
- **Signal access is not possible**
- **Embedding of the compliance channel and package, as well as application of the behavioral equalizer is required**
- **SigTest or custom software like DPOJET will perform the embedding and calculate measurements**



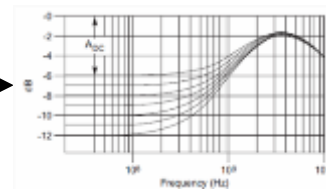
Signal Acquired  
from Compliance  
Board



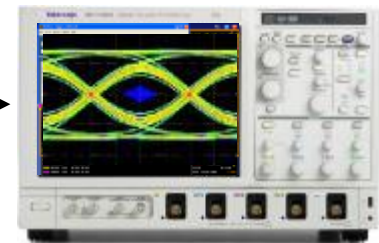
Embed Compliance  
Channel and Package



Closed Eye due to  
the Channel



Apply CTLE + DFE



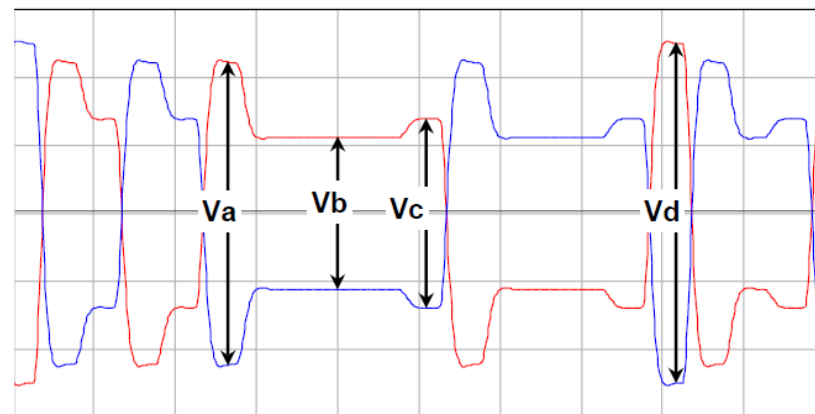
Open Eye for  
Measurements

# Compliance Equalization Presets



- Once in compliance mode, bursts of 100 MHz clock can be used to cycle through various settings of compliance presets to perform automated jitter, voltage, timing measurements.
- 11 presets for both PCIe 3.0 and PCIe 4.0 (22 total). All preset values must be supported by DUT.
- For Rx AIC testing, BER < 1E-12 while receiving any valid preset/TXEQ, or < 1E-4 while receiving either P7 or P8

Preset #	Preshoot (dB)	De-emphasis (dB)
P4	0.0	0.0
P1	0.0	-3.5 ± 1 dB
P0	0.0	-6.0 ± 1.5 dB
P9	3.5 ± 1 dB	0.0
P8	3.5 ± 1 dB	-3.5 ± 1 dB
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB
P5	1.9 ± 1 dB	0.0
P6	2.5 ± 1 dB	0.0
P3	0.0	-2.5 ± 1 dB
P2	0.0	-4.4 ± 1.5 dB
P10	0.0	Variable <sup>1</sup>



$$\begin{aligned}\text{De-emphasis} &= 20 \log_{10} V_b/V_a \\ \text{Preshoot} &= 20 \log_{10} V_c/V_b \\ \text{Boost} &= 20 \log_{10} V_d/V_b\end{aligned}$$

1. P10 levels are not fixed; its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used to test the boost level of the Tx during full swing

# PCIe 4.0 Overview



- Key attributes/requirements of PCIe 4.0
  - 16 GT/s, using scrambling, same as 8 GT/s, no encoding change
  - Reduction in RJ (random jitter) from 3ps (PCIe3) to ~1ps (PCIe4) for stressed eye parameters [PCIe Base Spec, Table 9-10]
  - Maintains backward compatibility w/ PCIe installed base of devices
  - Gen4 connector enhanced electrically
  - Behavioral Rx EQ data rate dependent
  - Limited channel: ~12" for 1 connector (including 4" AIC); requires use of repeater (both redriver & retimer) for longer channels and/or 2<sup>nd</sup> connector
  - New 'SRIS' independent RefClk modes
    - SRNS – Separate RefClk Independent with No SSC Architecture
    - SRIS – Separate RefClk Independent with SSC Architecture
  - New Rx Lane Margining feature measures EH/EW margin at end of channel
  - Eye height for Gen4 reduced to 15mVpp, Eye Width 0.3UI
- PCIe 4.0 0.9 Base spec draft finalized in June 2017
- PCIe 4.0 CEM Spec currently released at rev 0.5, draft 0.7 in process



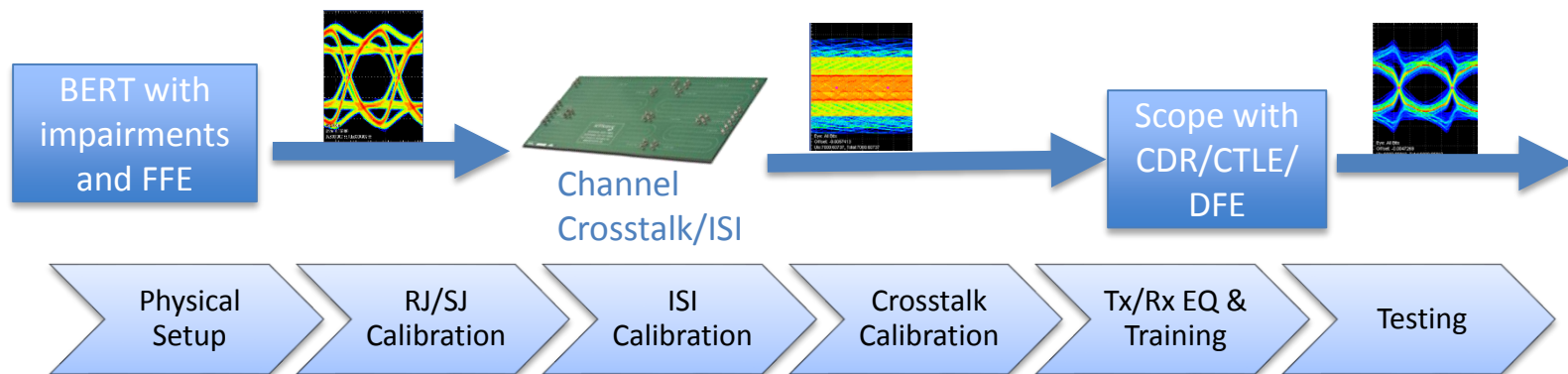
# PCIe 3.0/4.0 Tx Test Challenges



- **Can you quickly automate compliance testing?**
- **Transmitter margin dependent on channel and optimized equalizer settings.**
  - How will you verify actual transmitter margin meets design goals?
  - Can you accurately measure s-parameters and de-embed channel loss to properly characterize analog signal?
  - Do you have high speed probing capability to measure signal at point of interest?
- **Do you have PCIe-specific decoding capability for PCIe 1.0-4.0?**
  - Can you decode protocol messages for PCIe 1.0-4.0
  - If necessary can you apply CTLE/DFE and/or de-embed to analog protocol messages for debug
- **Server environments will require repeaters or re-timers, essential for signal transmission over long lossy channels. These IC's double the number of equalization combinations possible.**
  - How will you debug and perform interoperability test when repeaters/re-timers are present?
- **Do you have the tools for debug when compliance or interoperability tests fails (eg protocol decode, EQ optimization, s-parameter embed/de-embed, etc)**

# Receiver Test Overview

- Need fully integrated test system, including HW and SW solutions
  - Reliably put device under test into loopback mode
  - Facilitate link equalization training to optimize the channel, including built-in TXEQ and RXEQ optimization
  - Calibrate and sweep full suite of impairments (ISI, RJ, DMSI, CMI)
  - Debug DUT-specific problems with BER, FEC, and link training
- Solution must cover multiple speeds and spec generations (eg PCIe 3.0, PCIe 4.0, etc)



# New Challenges in Rx Testing

## PHY AND PROTOCOL-AWARE TEST AND DEBUG

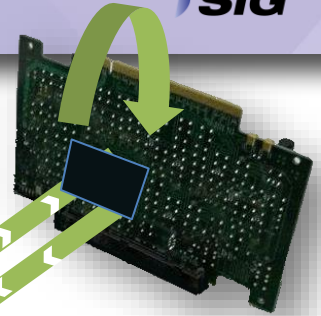


### Requires Protocol Awareness

1. Putting device into loopback
2. Performing link equalization

Pattern Generator with Stress

Error Counter



### Need Automated Solutions for Gen3 and Gen4 Standards

3. Easy setup of impaired signal
4. Auto calibration of stress impairments
5. Making accurate and repeatable BER measurements

### Go beyond compliance

6. Root-causing factors leading to bit-error or link training problems

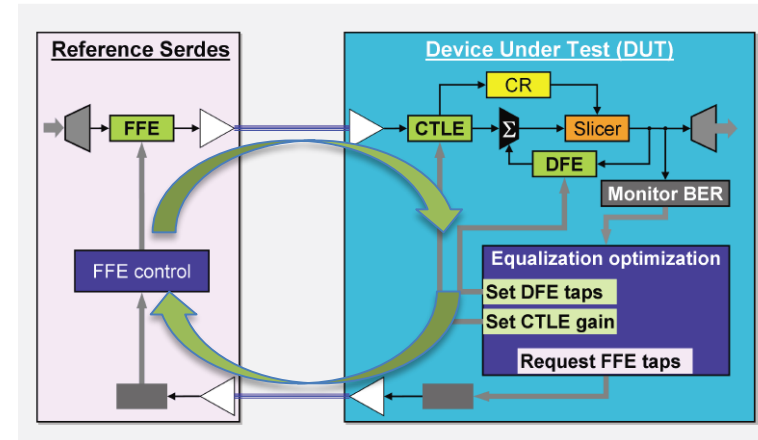
<b>ERROR BIT LOCATION</b>	<b>EXPECTED BIT</b>
200,457	0
1,247,356	1
1,447,890	0
3,885,245	0
4,001,876	1
8,233,191	0
...	

# New Challenges in Rx Testing

## PHY AND PROTOCOL-AWARE TEST AND DEBUG



- Entire link (including repeaters) requires link training capability.
  - Adaptive, optimizing equalization that requires coordination of Tx and Rx for each link at power up and recovery
  - Precise orchestration of FFE, CTLE, CR, slicer, and DFE functionality is essential,
  - Data stream/protocol management (scrambling, sequencing, encoding test patterns)
- NRZ (non-return to zero) symbol decoders/bit slicers with 15mVpp sensitivity.



# New Challenges in Rx Testing

## PHY AND PROTOCOL-AWARE TEST AND DEBUG



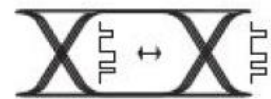
- Receiver margin testing requires **calibrated** insertion of various stresses for worst-case compliance testing:
  - Inter-Symbol Interference (ISI)
  - Random Jitter (RJ),
  - Common-Mode/Differential Mode Interference (CMI/DMI)
- Reference receiver models assist in calibrating compliance test conditions (eg Seasim/SigTest):
  - Models include the transmitted signal, applied stresses, and channel response to the receiver input pins
  - Calibration must be achieved through new Gen4 test fixtures
- Once PCIe 4.0 cal has been achieved, inject 100MHz SJ tone at 0.1UI and measure BER



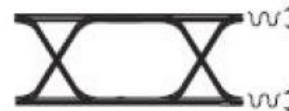
Random Jitter



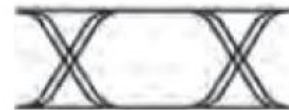
Sinusoidal Jitter



Bounded  
Uncorrelated Jitter



Sinusoidal  
Interference



F/2 Sub-Rate  
Clock Jitter



Inter-Symbol  
Interference

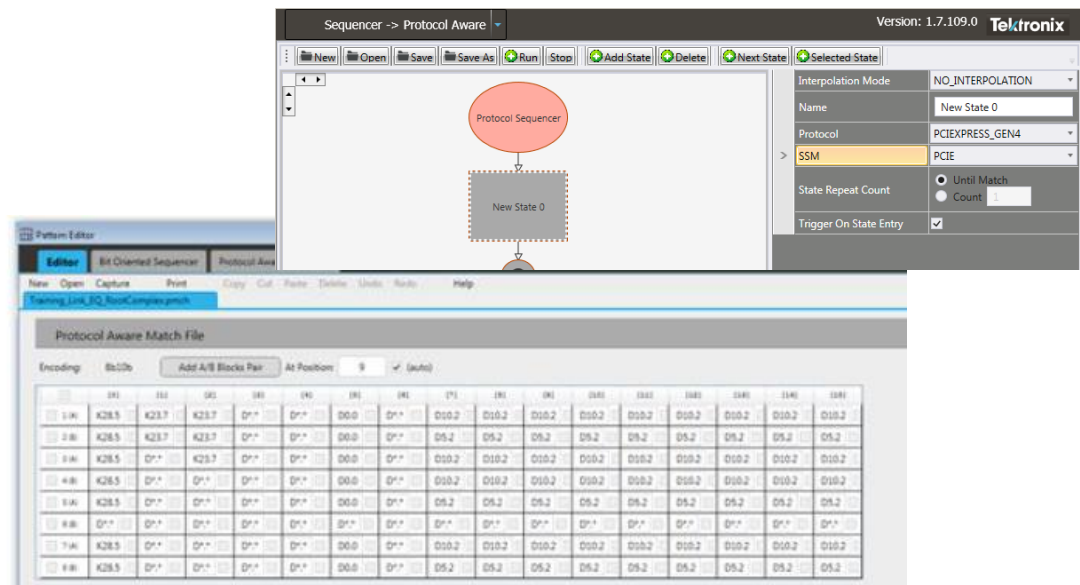
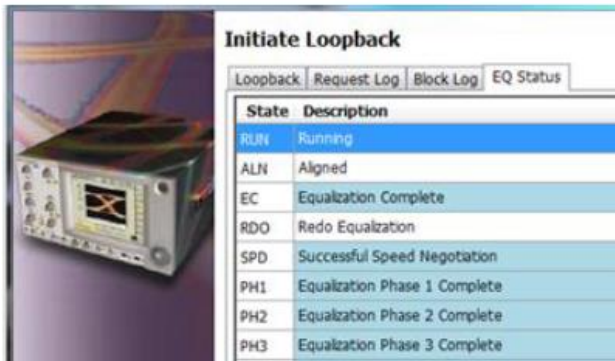
# PCIe 4.0 CEM Cal Procedure



- Calibrate Amplitude,  $R_j$ ,  $S_j$  @ 100MHz (1m cable to oscilloscope)
  - Amplitude = 800mVpp
  - $R_j = 1\text{ps RMS}$
  - $S_j @ 100\text{MHz} = 0.1\text{UI}$
- Establish 30dB, 28dB and 27dB channels
- Vary the CBB Variable ISI Pair
- BERT -> 1m SMA cable -> Variable ISI brd -> 1 foot SMP cable -> CBB Rx Lane0 -> CLB Tx Lane0 -> 1ft SMP cable -> Variable ISI brd -> 1m SMA cable to Scope (embedding refpkg model)
- Calibrate DMI (14mV) and CMI (150mV) @ end of channel
- **Find Optimal Tx EQ Preset (27db channel)**
- **Increase channel loss from 27 -30dB using the Variable ISI board**
- Find loss where EW/EH drop below targets and step back one pair
- Ensure Preset is still optimal
- **Vary the following until EW(18.75 +/-0.5)/EH (15mV +/-1.5) targets are met**
  - $S_j$  (5-10ps)
  - DMI (10-25mV)
  - Amplitude (720-800mV)
- Record Final Settings

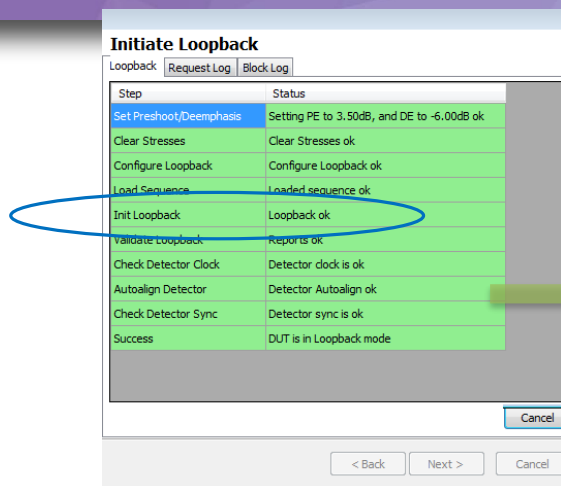
# Debugging Handshaking Issues

- Two phase link equalization for PCIe 3.0/--complete 8G link eq, then begin 16G link eq
- BERT displays LTSSM status and logs
- Pattern/protocol sequencer/editor enables real-time editing of handshaking flow
- Programmable BERT detector pattern matching allows creation of customized handshaking for debugging transitions





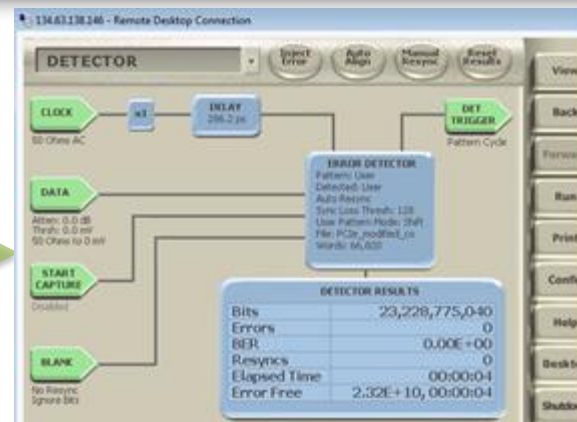
# Compliance Workshop Use Case— PCIe 4.0 Broadcom AIC DUT



*Sequencer Loaded for PCIe  
Loopback Initiation and  
Debug—PCIe 3.0 -> PCIe 4.0*



*Iterative requests  
from the DUT for  
TXEQ tuning*



*LTSSM Recovery loopback achieved  
and BER SJ stress test initiated*

**Special thanks  
to Broadcom  
Ft Collins  
team for their  
collaboration!**



*BERT Debug tools observed  
protocol traffic to identify  
handshaking issues*

*DUT initial preset was modified  
based on feedback from BERT to  
facilitate LTSSM Recovery loopback*



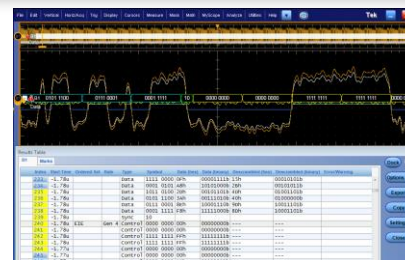
# Scope Tx Decoder for PCIe 1.0-4.0



- Decodes and displays PCIe data using characters and names that are familiar from the standard, such as:
  - SKP
  - Electrical Idle
  - EIEOS
- Easily configured through “Bus Setup” under “Vertical” menu with a variety of user-adjustable settings
- Results table shows time-correlated listing of events time-correlated with waveform view
- Integrated search with marks
- BERT protocol/pattern match can be used to cross-trigger scope, which can use Tx Decoder for Tx/Rx link training test and debug
- Serial triggering for debug available for PCIe 1.0-2.0



# CEM-based Tx/Rx LinkEQ

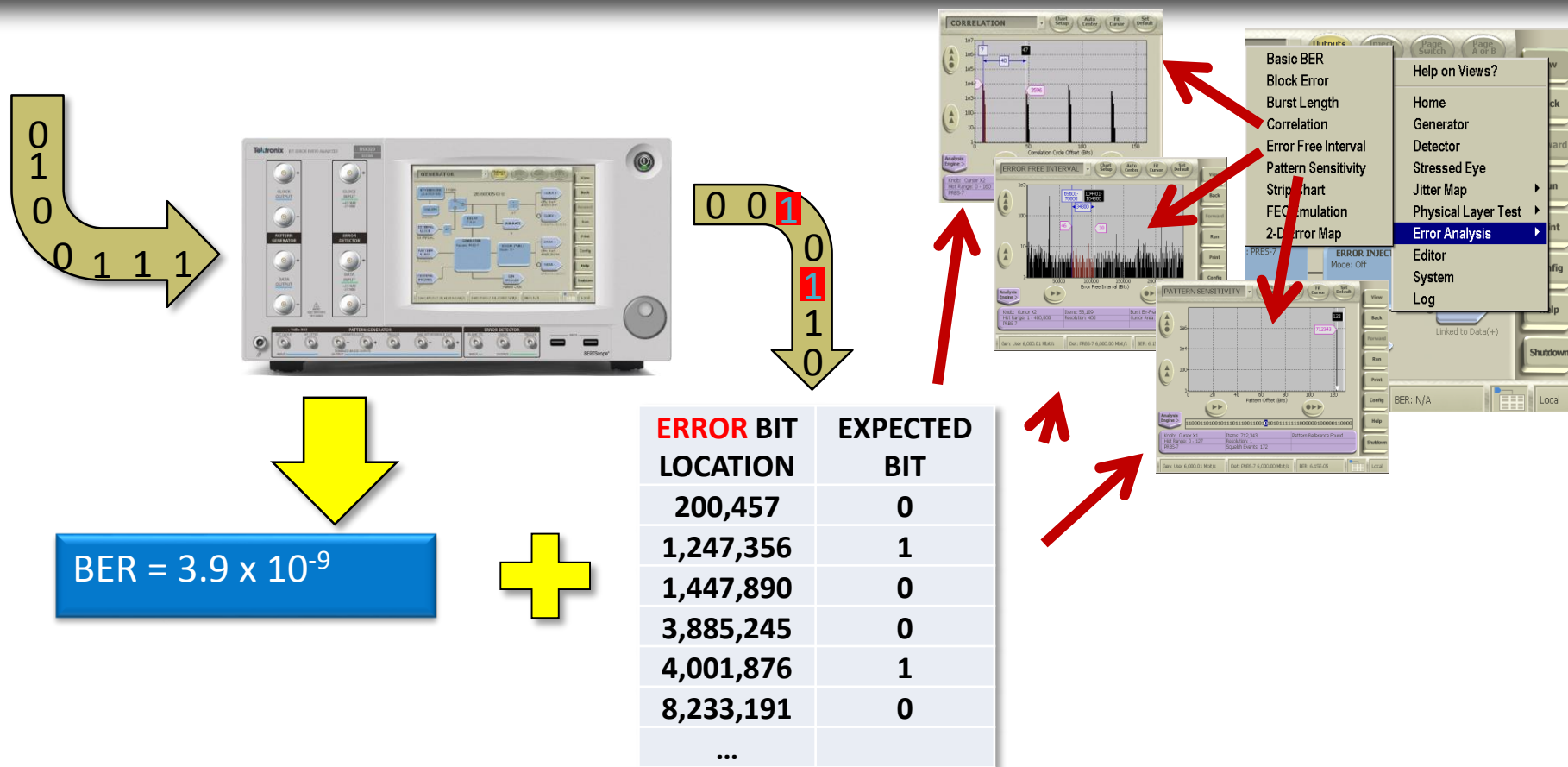


- BERT sends trigger to scope based on customizable protocol message match
- BERT and DUT negotiate through Link EQ by optimizing TxEQ from BSX
- BERT uses LTSSM to train DUT's transmitter
- BERT uses handshaking to put DUT into loopback
- PCIe compliance requirement (at workshops), debug often required



- Scope decodes PCIe 1.0-4.0 protocol messages
- Scope verifies DUT has actually implemented the preset/EQ that it claims to have done
- DUT must “train up” in speed—PCIe 1.0, 2.0, 3.0, 4.0
- Scope verifies handshaking was performed in <500ns

# Debugging Physical Layer Issues



Knowing *error locations* points to *Error Patterns* which lead to unique debugging information. This allows you to “virtually probe” inside your DUT

- **New PCIe 4 test challenges in protocol handshaking require new test and debug tools**
- **Multiple iterative steps are often required to put PCIe 4 DUT's into loopback**
- **Debug requires precise orchestration of multiple aspects, including equalization, protocol messaging, clocking, and signal integrity**

**Thank you for attending the  
PCI-SIG Developers Conference  
Asia-Pacific Tour 2017.**

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